

ABSTRACT OF THE DISCLOSURE

5 A bus control module as a terminal stage for a multi-stage clock/alarm distribution scheme used in a signaling server organized into a plurality of uniquely addressable shelves. The signaling server includes a system timing generator, one or more clock distribution modules arranged in a nested hierarchical manner, and a plurality of bus control modules, wherein each bus control module interfaces with at least a portion of line cards disposed in a shelf. The system timing generator provides a framed serial control signal, SFI, for controlling the operation of the multi-stage clock/alarm distribution scheme. The SFI signal encodes the IDs of the clock distribution modules and bus control modules whereby a system clock generated by the system timing generator based on a select reference input is successively fanned-out by the intermediate clock distribution modules based on address and ID information encoded in select fields of the SFI frames until the fanned-out system clocks are received by the bus control modules. Thereafter, each bus control module provides a copy of the system clock to the line cards controlled by it based on the SFI signal. The bus control module also collects various alarms and status signals from the line interface cards to be multiplexed into a framed serial signal, EAS, based on its ID, which is transmitted upstream to the system timing generator for further

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